1. *Course number and name*
   ENGR 378: Digital System Design

2. *Credits and contact hours*
   3 credit hours; one 100-minute lecture session/week and one 2-hour-45-minute lab session/week

3. *Instructor's or course coordinator's name*
   Instructor: Hamid Mahmoodi, Professor of Electrical and Computer Engineering
   Course coordinator: Hamid Mahmoodi, Professor of Electrical and Computer Engineering

4. *Text book, title, author, and year*
   Charles H. Roth, Jr, *Digital Systems Design Using Verilog*, Cengage Learning, 2016

   a. *other supplemental materials*
      (none)

5. *Specific course information*
   a. *brief description of the content of the course (catalog description)*
      CMOS digital circuits and their electrical properties. Logic circuit design with functional units. Algorithmic sequential machine design. Design with programmable logic devices. Hardware description and simulation language.

   b. *prerequisites or co-requisites*
      grade of C- or better in ENGR 356

   c. *indicate whether a required, elective, or selected elective course in the program*
      Required for Computer Engineering; elective for Electrical Engineering.

6. *Specific goals for the course*
   a. *specific outcomes of instruction, ex. The student will be able to explain the significance of current research about a particular topic.*
   - The student will demonstrate an ability to analyze combinational and sequential circuits.
   - The student will demonstrate an ability to design combinational and sequential circuits.
   - The student will demonstrate knowledge of structural, dataflow, and behavioral modeling of digital system.
   - The student will demonstrate knowledge of Hardware Description Language (HDL) for digital system design and simulation.
   - The student will demonstrate a skill in using software tools.
   - The student will demonstrate a working knowledge of programmable logic devices
   - The student will demonstrate a skill in using tools for digital design with programmable logic devices.

b. explicitly indicate which of the student outcomes listed in Criterion 3 or any other outcomes are addressed by the course.
Course addresses ABET Student Outcome(s): a, b, c, e, k.

7. Brief list of topics to be covered

- Introduction to Verilog HDL
- Basic methods for circuit specification
- Programmable logic devices and FPGA's
- Design and specification of simple circuits
- Arithmetic unit design
- State Machine design
- SM Charts
- Design with FPGAs
- Lab: Computer-aided design and simulation tools; digital circuit verification and troubleshooting, synthesis and implementation to FPGA