1. **Course number and name**
   
   ENGR 851: Advanced Microprocessor Architectures

2. **Credits and contact hours**
   
   3 credit hours; one 2-hour-45-minute lecture sessions/week

3. **Instructor’s or course coordinator’s name**
   
   Instructor: Seapahn Megerian, Ph.D.
   
   Course coordinator: Hamid Mahmoodi, Assistant Professor of Computer Engineering

4. **Text book, title, author, and year**
   

   a. other supplemental materials
      
      Lecture notes

5. **Specific course information**
   
   a. brief description of the content of the course (catalog description)
      
      Microprocessor architecture and register organization. Multiprogramming, process scheduling and synchronization, and multitasking. Memory management and privileged machine states. Examples of 32-bit machines. Reduced architectures: RISC approach, MIPS

   b. prerequisites or co-requisites
      
      ENGR 456

   c. indicate whether a required, elective, or selected elective course in the program
      
      Elective for Electrical Engineering.

6. **Specific goals for the course**
   
   a. specific outcomes of instruction, ex. The student will be able to explain the significance of current research about a particular topic.
      
      - The student will be able to describe performance metrics of microprocessors
      - The student will be able to explain RISC, CISC, and Stack processors
      - The student will be able to describe multithreading and parallel programming
      - The student will be able to perform pipelining and identify hazards
      - The student will be able to describe ILP, VLIW, Superscalar, and dynamic scheduling
      - The student will be able to analyze and design memory hierarchy
      - The student will be able to design branch prediction and speculation

   b. explicitly indicate which of the student outcomes listed in Criterion 3 or any other outcomes are addressed by the course.
      
      Course addresses ABET Student Outcome(s): a, b, c, d, e, g, i, j, k.
7. Brief list of topics to be covered

- Background review; performance metrics
- RISC, CISC, Stack Processors, etc; Performance and reliability calculations
- Multithreading and parallel programming; Parallel algorithms
- Pipelining and hazards
- ILP, VLIW, Superscalar, and dynamic scheduling
- Superscalar continued - register renaming
- Memory hierarchy, caching, and analysis
- Branch prediction and speculation
- Advanced topics