1. Course number and name
   **ENGR 856: Nano-Scale Circuits and Systems**

2. Credits and contact hours
   3 credit hours; one 2-hour-45-minute lecture sessions/week

3. Instructor's or course coordinator's name
   Instructor: Hamid Mahmoodi, Assistant Professor of Computer Engineering
   Course coordinator: Hamid Mahmoodi, Assistant Professor of Computer Engineering

4. Text book, title, author, and year
   Optional:
   - Leakage in Nanometer CMOS Technologies, S. G. Narendra and A. Chandrakasan, Springer © 2005

   a. other supplemental materials
      - Lecture notes
      - Conference/journal papers

5. Specific course information
   a. brief description of the content of the course (catalog description)
      Advanced topics in VLSI device, circuit and system design including high-performance and low-power design issues, challenges of technology scaling, technologies and solutions at different levels of abstraction. Requires class project.

   b. prerequisites or co-requisites
      ENGR 453 or equivalent

   c. indicate whether a required, elective, or selected elective course in the program
      Elective

6. Specific goals for the course
   a. specific outcomes of instruction, ex. The student will be able to explain the significance of current research about a particular topic.
      - The student will have the knowledge of silicon technology scaling and trends
      - The student will have the knowledge of challenges of technology scaling in nano-scale regimes
      - The student will be able to apply low power design approaches and techniques at different levels of abstraction
      - The student will have the knowledge of challenges associated leakage currents and process variations
      - The student will be able to develop a new design techniques under excessive leakage and process variations
• The student will be able to exploiting non-classical CMOS devices for circuit
design in such technologies
• The student will have the knowledge of prospects of future non-silicon
nanotechnologies

b. explicitly indicate which of the student outcomes listed in Criterion 3 or any other
outcomes are addressed by the course.
Course addresses ABET Student Outcome(s): a, b, c, d, e, g, i, j, k.

7. Brief list of topics to be covered
• Technology scaling and trends
• CMOS scaling challenges in sub 100nm regimes
• Low power design
• Energy recovery techniques
• Techniques for leakage power reduction
• Process variations in devices and interconnects
• Circuit design in nano-scaled technologies
• Self-timed circuits
• High speed VLSI arithmetic units
• Emerging memory technologies
• SOI technology and circuits
• Emerging non-silicon nanotechnologies